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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,771	12/02/2003	Arun Rao	15144US02	3834
23446 7590 09/29/2009 MCANDREWS HELD & MALLOY, LTD 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661			EXAMINER COLUCCI, MICHAEL C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/725,771

Applicant(s)

RAO ET AL.

Examiner

MICHAEL C. COLUCCI

Art Unit

2626

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 20 and 24-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20 and 24-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 07/06/2009 have been fully considered but they are not persuasive.

Argument (Remarks pages 3 and 4):

- Art not teaching *"a memory for storing results of the Huffman decoding of the frame of encoded audio data, the results of the prediction decoding of the encoded audio frame, and the results of intensity coupling the frame of encoded audio data, wherein the results of the prediction decoding for the frame of encoded audio data at least partially overwrite the results of the Huffman decoding of the frame of encoded audio data, and wherein the results of the intensity coupling for the frame of encoded audio data at least partially overwrite the results of the prediction decoding of the frame of encoded audio data"*

Response to argument:

Re Araki in view of Kodama not teaching *"a memory for storing results of the Huffman decoding of the frame of encoded audio data, the results of the prediction decoding of the encoded audio frame, and the results of intensity coupling the frame of encoded audio data, wherein the results of the prediction decoding for the frame of encoded audio data at least partially overwrite the results of the Huffman decoding of the frame of encoded audio data, and wherein*

the results of the intensity coupling for the frame of encoded audio data at least partially overwrite the results of the prediction decoding of the frame of encoded audio data", Examiner would first like to point out the identical nature of Araki with the present invention. Araki explicitly and identically teaches a well known advanced audio coding method (AAC), wherein Fig. 2 of Araki explicitly teaches elements 2-9 as a multiplexing version of the present invention Fig. 3. The present invention teaches a de-multiplexing routine which is merely a reverse operation of multiplexing. Araki alone teaches coding operation with a Huffman code table (Araki [0013]). Regardless, Examiner has still incorporated Kodama to address what is well known, wherein Kodama teaches Huffman decoding (Kodama Fig. 3 element 40) identical to the present invention (present invention drawings Fig. 3 element 410).

Consider the present inventions support for partially overwriting data, merely states "audio decoding buffers may be carried out by monitoring memory usage during the program operation, analyzing memory allocation, *determining data which may be overwritten*, and calculating the minimum amount of memory (present invention spec. [0093]). Given this support, the act of partially overwriting data is merely construed as the act of partially overwriting data as is demonstrated by Kodama (Kodama Fig. 5).

Consider the memory writing operations of Kodama, wherein a memory address is overwritten constantly. Though it may be obvious that partially overwriting memory is well known, Examiner will maintain the use of Kodama. Kodama gives a clear explanation of the well established use of partial memory

overwriting, wherein various portions of an address memory are overwritten between specific operations such as TNS, filter bank, block switching, etc. The time axis is demonstrated vertically and the memory address horizontally, showing the amount of memory effected with respect to time.

Kodama goes on to state examples such as in the case where data is present which is not used in the noiseless decoding at the next stage, and which should be conserved to be used at the processing at the latter stage out of data generated at the bit stream decoding, an instruction is sent from the general purpose processor 10 to the DMA controller 15 to be saved in the external memory 1 immediately after the bit stream decoding. By doing so, the saved region can be used as a new data region immediately after the noiseless decoding.

Thereafter, in the same manner, the general purpose processor 10 is controlled in such a manner that when the k-th processing is started, the content of the data memory 14 unnecessary for the k-th processing out of the k-1-th processing results is saved in the external memory 1, the instruction group required for the k+1-th processing and data are transferred to the instruction memory 13 and data memory 14 from the external memory 1. As a consequence, the audio coprocessor 11 is capable of decreasing the memory capacity required for performing audio processing with respect to the audio streams. Incidentally, symbol k denotes an arbitrary integer.

FIG. 5 shows an example of time transition of the data memory 14 in the MPEG-2 AAC decoding processing. In FIG. 5, the horizontal axis denotes a

memory address while the vertical axis denotes time, respectively. Furthermore, the point shown by a black round mark denotes a start time of each processing while the black square mark denotes a start time of the DMA transfer. A graph shown in FIG. 5 shows which data in the processing from which time up to which time occupies which address space in the data memory 14. Consequently, FIG. 5 is a view showing a state transition of the memory space in the data memory 14 along with the transition of the processing (Kodama [0072]-[0074] & Fig. 3 and 5).

This overwriting method can easily be implemented between the decoding, intensity coupling, and prediction stages of Araki in the same manner it is implemented in Kodama.

Thus, there is motivation for combining the well known teachings of Araki (Araki Fig. 2) with the memory overwriting methods as taught by Kodama (Kodama [0072]-[0074] & Fig. 3 and 5).

Examiner has provided similar more explicit explanation and motivation to better define the memory overwriting operation that may not be easily identifiable based on Fig. 3 of alone. See rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 20-22, 24-26, 28, 29, 31, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki US 20020022898 A1 (hereinafter Araki) in view of Kodama US 20020013633 A1 (hereinafter Kodama).

Re claims 20 and 28, Araki teaches a system for decoding an audio signal, said system comprising:

one or more audio decoding circuits for performing one or more functions on a frame of encoded audio data, wherein the one or more audio decoding circuits ([0012] & Fig. 2) comprise;

a Huffman decoder for Huffman decoding the frame of encoded audio data ([0012-0013] & Fig. 2 item 10); misspoken

a prediction decoder for prediction decoding the frame of encoded audio data ([0012-0013] & Fig. 2 item 6); and

an intensity coupling circuit for intensity coupling the frame of encoded audio data ([0012-0013] & Fig. 2 item 5)

a memory for storing results of the Huffman decoding of the frame of encoded audio data, the results of the prediction decoding of the encoded audio frame, and the results of intensity coupling the frame of encoded audio data, wherein the results of the prediction decoding for the frame of encoded audio data at least partially overwrite the results of the Huffman decoding of the frame of encoded audio data, and wherein the results of the intensity coupling for the frame of encoded audio data at least partially overwrite the results of the

prediction decoding of the frame of encoded audio data ([0012-0013] & Fig. 2 transition from item 6 to item 10).

However, Araki fails to teach results of the intensity coupling for the frame of encoded audio data at least partially overwrite the results of the prediction decoding

Kodama states examples such as in the case where data is present which is not used in the noiseless decoding at the next stage, and which should be conserved to be used at the processing at the latter stage out of data generated at the bit stream decoding, an instruction is sent from the general purpose processor 10 to the DMA controller 15 to be saved in the external memory 1 immediately after the bit stream decoding. By doing so, the saved region can be used as a new data region immediately after the noiseless decoding.

Thereafter, in the same manner, the general purpose processor 10 is controlled in such a manner that when the k-th processing is started, the content of the data memory 14 unnecessary for the k-th processing out of the k-1-th processing results is saved in the external memory 1, the instruction group required for the k+1-th processing and data are transferred to the instruction memory 13 and data memory 14 from the external memory 1. As a consequence, the audio coprocessor 11 is capable of decreasing the memory capacity required for performing audio processing with respect to the audio streams. Incidentally, symbol k denotes an arbitrary integer.

FIG. 5 shows an example of time transition of the data memory 14 in the MPEG-2 AAC decoding processing. In FIG. 5, the horizontal axis denotes a

memory address while the vertical axis denotes time, respectively. Furthermore, the point shown by a black round mark denotes a start time of each processing while the black square mark denotes a start time of the DMA transfer. A graph shown in FIG. 5 shows which data in the processing from which time up to which time occupies which address space in the data memory 14. Consequently, FIG. 5 is a view showing a state transition of the memory space in the data memory 14 along with the transition of the processing (Kodama [0072]-[0074] & Fig. 3 and 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Araki to incorporate results of the intensity coupling for the frame of encoded audio data at least partially overwrite the results of the prediction decoding as taught by Kodama to allow for an audio processing method capable of decreasing the memory capacity required for performing audio processing with respect to the audio streams (Kodama [0072]-[0074] & Fig. 3 and 5).

Re claims 24 and 31, Araki teaches the system of claim 22, wherein the one or more audio decoding circuits further comprise a filter bank ([0012-0013] & Fig. 2 item 3)

Re claims 25 and 32, Araki teaches the system of claim 22, wherein the one or more circuits further comprises a temporal noise shaper ([0012-0013] & Fig. 2 item 4)

Re claim 26, Araki teaches a system for decoding an audio signal, said system comprising:

a first audio decoding circuit for performing a first audio function on a frame of encoded audio data ([0012-0013] & Fig. 2), wherein the first audio decoding circuit is selected from a group consisting of an inverse quantizer for inverse quantizing the frame of encoded audio data, a bitstream demultiplexer for demultiplexing the frame of encoded audio data, and a filter bank for filtering the frame of encoded audio data;

a second audio decoding circuit for performing a second audio function on a frame of encoded audio data, wherein the second audio decoding circuit is selected from a group consisting of a bitstream demultiplexer for demultiplexing the frame of encoded audio data a filter bank for filtering the frame of encoded audio data, and an intensity coupler for intensity coupling the frame of encoded audio data a memory for storing outputs of the first audio decoding circuit ([0012-0013] & Fig. 2)

However Araki fails to teach the first audio decoding circuit is selected from a group consisting of an *inverse quantizer for inverse quantizing* the frame of encoded audio data, a bitstream demultiplexer for demultiplexing the frame of encoded audio data, and a filter bank for filtering the frame of encoded audio data

wherein the memory stores the outputs of the second audio decoding circuit on the frame over at least a portion of the results of the first audio decoding circuit on the frame

Kodama teaches (like the present invention [0019]) an instruction memory, wherein Kodama teaches the instruction memory 13 stores an instruction code with respect to the general purpose processor 10. Furthermore, the data memory 14 stores various data to be processed by the general purpose processor 10. Furthermore, the general purpose processor 10 performs processing in accordance with the instruction code stored in the instruction memory 13. In the embodiment, the general purpose processor 10 captures and buffers the data (audio streams) primarily required in the audio coprocessor 11. Then, the general purpose processor 10 fetches data such as various tables, a filter bank coefficient and the like corresponding to the progress stage of the audio data reconstruction processing, and delivers the data to the audio coprocessor 11. Further, the general purpose processor 10 stores data obtained by the audio coprocessor 11 in the data memory 14, and controls the DMA controller 15 (Kodama [0034-0035]).

Further, Kodama demonstrates a demultiplexing routine nearly identical to that of the present invention with the exception of prediction being shown (Kodama Fig. 3 items 42 and 40), wherein Kodama furthermore teaches two memories present which write information back and forth based on the function of each stage of Fig. 3 (Kodama Fig. 4a and 4B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Araki to incorporate the first audio decoding circuit is selected from a group consisting of an inverse quantizer for inverse quantizing the frame of encoded audio data, a bitstream demultiplexer for demultiplexing the frame of encoded audio data, and a filter bank for filtering the frame of encoded audio data, wherein the memory stores the outputs of the second audio decoding circuit on the frame over at least a portion of the results of the first audio decoding circuit on the frame as taught by Kodama to allow for the progressive retrieval of data at various stages during an audio (i.e. MPEG-2, etc.) demultiplexing routine, wherein audio data can be freely captured relative to an instruction memory that transfers information along a series of functions (i.e. prediction, gain, quantization, Huffman/noiseless, etc.) (Kodama [0034-0035]).

Re claim 27, Araki teaches the system of claim 26, wherein the first audio decoding circuit comprises a filter bank for filtering the frame of encoded audio data and wherein the second audio decoding circuit comprises a bitstream demultiplexer ([0012-0013] & Fig. 2 item 5), and further comprising:

However, Araki fails to teach wherein the memory stores the output of the intensity coupler over at least a portion of the results of the second audio decoding circuit

Kodama teaches (like the present invention [0019]) an instruction memory, wherein Kodama teaches the instruction memory 13 stores an instruction code

with respect to the general purpose processor 10. Furthermore, the data memory 14 stores various data to be processed by the general purpose processor 10. Furthermore, the general purpose processor 10 performs processing in accordance with the instruction code stored in the instruction memory 13. In the embodiment, the general purpose processor 10 captures and buffers the data (audio streams) primarily required in the audio coprocessor 11. Then, the general purpose processor 10 fetches data such as various tables, a filter bank coefficient and the like corresponding to the progress stage of the audio data reconstruction processing, and delivers the data to the audio coprocessor 11. Further, the general purpose processor 10 stores data obtained by the audio coprocessor 11 in the data memory 14, and controls the DMA controller 15 (Kodama [0034-0035]).

Further, Kodama demonstrates a demultiplexing routine nearly identical to that of the present invention with the exception of prediction being shown (Kodama Fig. 3 items 42 and 40), wherein Kodama furthermore teaches two memories present which write information back and forth based on the function of each stage of Fig. 3 (Kodama Fig. 4a and 4B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Araki to incorporate the memory stores the output of the intensity coupler over at least a portion of the results of the second audio decoding circuit as taught by Kodama to allow for the progressive retrieval of data at various stages during an audio (i.e. MPEG-2, etc.) demultiplexing routine, wherein audio data can be freely captured relative to an

instruction memory that transfers information along a series of functions (i.e. prediction, gain, quantization, Huffman/noiseless, etc.) (Kodama [0034-0035]).

Re claim 29, Araki teaches the method of claim 28, further comprising:

Huffman decoding the frame of encoded audio data ([0012-0013] & Fig. 2 item 10);

However, storing results of Huffman decoding the encoded audio data in the memory over at least another portion of the results of the one or more audio decoding functions comprising decoding ([0012-0013] & Fig. 2 transition from item 6 to item 10, merely replacing data after adjustment).

Re claim 30, Araki teaches the system of claim 22, wherein the one or more audio decoding circuits further comprises an intensity coupling circuit ([0012-0013] & Fig. 2 item 5).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Colucci whose telephone number is (571)-270-1847. The examiner can normally be reached on 9:30 am - 6:00 pm, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richemond Dorvil can be reached on (571)-272-7602. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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